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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,152	06/01/2007	Hideki Nakahara	50478-3900	7767

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EXAMINER	
NGUYEN, LEON VIET Q	
ART UNIT	PAPER NUMBER
2611	
MAIL DATE	DELIVERY MODE
08/24/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,152	NAKAHARA ET AL.	
	Examiner	Art Unit	
	LEON-VIET Q. NGUYEN	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15,16 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-23* is/are allowed.

6)☒ Claim(s) *1-13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/30/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 8/30/06 was filed after the mailing date of 8/30/06. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. Figures 2-4, 6-12 and 37 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 2, 5-9, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (hereinafter referred to as AAPA) in view of Takeda et al (US4551846).

Re claim 1, AAPA teaches a clock recovery circuit for recovering a symbol clock from an input signal, comprising:

an N-interval detection unit (circuit 3700 in fig. 37) operable to detect an N zero-crossing interval (page 4 lines 4-6);

a judgment unit (generator 3701 in fig. 37) operable to judge whether the N zero-crossing interval is within a predetermined interval range (page 4 lines 7-10); and

a clock generation unit (symbol clock 128 in fig. 4) operable to generate a symbol clock based on a result of the judgment (page 3 lines 2-7).

AAPA fails to teach to detecting an N zero-crossing interval with reference to N+1 zero-crossing signals obtained from the input signal, where N is an integer greater than or equal to 2. However Takeda teaches detecting an N zero-crossing interval (col. 3 lines 45-46) with reference to N+1 zero-crossing signals obtained from the input signal (col. 1 lines 39-41, since the intervals are counted between successive zero-crossing points it would be necessary to have one more zero-crossing point than zero-crossing intervals), where N is an integer greater than or equal to 2 (col. 3 lines 47-49).

Therefore taking the combined teachings of AAPA and Takeda as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of Takeda into the circuit of AAPA. The motivation to

combine Takeda and AAPA would be to increase the signal to noise ratio (col. 3 lines 50-52 of Takeda).

Re claim 2, the modified invention of AAPA teaches a clock recovery circuit wherein the clock generation unit uses the N+1 zero-crossing signals as valid zero-crossing signals in generating the symbol clock if judged in the affirmative (page 3 lines 16-22 of AAPA), and ignores at least one of the N+1 zero-crossing signals in generating the symbol clock if judged in the negative (page 4 lines 22-26 of AAPA).

Re claims 5 and 6, the modified invention of AAPA teaches a clock recovery circuit wherein N=2 (col. 3 lines 45-50 of Takeda, it would be obvious to set N to 2). Furthermore, it would be a designer's choice to set the minimum and maximum time interval which would yield the most optimal results.

Re claim 7, the modified invention of AAPA teaches a clock recovery circuit, wherein the N-interval detection unit includes:

a zero-crossing detection subunit operable to detect zero crossings based on the input signal (col. 9 lines 17-19 of Takeda, it would be obvious to detect the zero-crossings before counting the zero-crossing intervals);

a counting subunit operable to measure a time interval between adjacent zero crossings (col. 9 lines 8-12 of Takeda); and

an adding subunit operable to sum N number of adjacent intervals, and output the result as an N-interval control signal (col. 9 lines 12-16 of Takeda).

Re claim 8, modified invention of AAPA teaches a clock recovery circuit wherein the input signal is an in-phase or quadrature component of a signal obtained by detecting a modulated signal (page 1 lines 25-28 of AAPA).

Re claim 9, the modified invention of AAPA teaches a clock recovery circuit further comprising:

a 1-interval detection unit operable to detect a 1 zero-crossing interval between adjacent zero-crossings (col. 1 lines 39-41 of Takeda), wherein

the judgment unit judges whether the 1 zero-crossing interval is within a predetermined interval range (page 4 lines 7-10 of AAPA), and only judges in the affirmative if the 1 zero-crossing interval and the 2 zero-crossing interval are both within respective predetermined interval ranges (page 4 lines 16-22 of AAPA).

Re claim 15, the claimed limitations recited have been analyzed and rejected with respect to claims 1 and 9.

Re claim 16, it would be a designer's choice to set the minimum and maximum time interval which would yield the most optimal results.

3. Claims 3, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (hereinafter referred to as AAPA) and Takeda et al (US4551846) in view of Kim (US5859671).

Re claim 3, the modified invention of AAPA fails to teach a clock recovery circuit wherein the clock generation unit includes a circuit operable to adjust a timing of the generated symbol clock based on a phase error with a valid zero-crossing signal, and output the adjusted symbol clock.

However Kim teaches a clock recovery circuit (fig. 1, col. 1 line 38) wherein the clock generation unit includes a circuit operable to adjust a timing of the generated symbol clock (block 60 in fig. 1, col. 1 lines 49-51) based on a phase error (block 50 in fig. 1, col. 1 lines 49-51), and output the adjusted symbol clock (the output of block 60 in fig. 1). It would have been obvious to use the phase error with a valid zero-crossing signal as taught by AAPA (see page 2 lines 5-7 of AAPA).

Therefore taking the modified teachings of AAPA and Takeda with Kim as a whole, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to incorporate the feature of Kim into the circuit of AAPA and Takeda. The motivation to combine Kim, Takeda and AAPA would be to demodulate a transmission signal without an error (col. 1 lines 33-36 of Kim).

Re claim 10, the claimed limitations recited have been analyzed and rejected with respect to claim 3.

Re claim 12, the claimed limitations recited have been analyzed and rejected with respect to claims 1-3. Furthermore, it would be necessary to have I and Q component processing units to process received I and Q signals (see page 1 line 25 – page 2 line 8 of AAPA).

Re claim 13, the modified invention of AAPA teaches a clock recovery circuit

wherein the modulated signal has a frame structure that includes a preamble, a unique word and data (page 1 lines 14-16 of AAPA), and

the clock recovery circuit further comprises a switching circuit (switch 3706 in fig. 37 of AAPA) operable to output zero-crossing signals validated by the processing units to the clock generation unit as phase error information when the detected signal corresponds to one of the preamble and the unique word (page 4 lines 10-15 of AAPA), and to output the zero-crossing signals obtained from the in-phase and quadrature signals to the clock generation unit as phase error information when the detected signal corresponds to the data (page 1 line 25 – page 2 line 8 of AAPA).

4. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (hereinafter referred to as AAPA) and Takeda et al (US4551846) in view of Bolger et al (US5565930).

Re claim 4, the modified invention of AAPA fails to teach a clock recovery circuit wherein the clock generation unit includes a circuit operable to generate a pulse at a center of adjacent zero crossings with reference to a valid zero-crossing signal, adjust a timing of the generated symbol clock based on a phase error with the generated pulse, and output the adjusted symbol clock.

However Bolger teaches a circuit operable to generate a pulse at a center of adjacent zero crossings with reference to a valid zero-crossing signal (col. 9 lines 38-45), adjust a timing of the generated symbol clock (col. 9 lines 45-48), and output the adjusted symbol clock (the output of circuit 30 in fig. 4). It would be obvious that to use the phase error associated with the generated pulse to adjust the timing.

Therefore taking the modified teachings of AAPA and Takeda with Bolger as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of Bolger into the circuit of AAPA and Takeda. The motivation to combine Bolger, Takeda and AAPA would be to increase the bit resolution (col. 3 lines 16-18 of Bolger).

Re claim 11, the claimed limitations recited have been analyzed and rejected with respect to claim 4.

Allowable Subject Matter

5. Claims 21-23 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: The allowable subject matter in claim 21 pertains to a center detection subunit operable to detect a temporal position of a center between adjacent in-phase and adjacent quadrature zero-crossing signals, and output in-phase center signals and quadrature center signals;

a M-interval judgment subunit operable to judge whether each in-phase and quadrature interval signal is within a predetermined interval range;

a N-interval judgment subunit operable to sum two adjacent in-phase interval signals and N adjacent quadrature interval signals to generate an in-phase N-interval signal and a quadrature N-interval signal, and judge whether each in-phase and quadrature N-interval signal is within a predetermined interval range (N, M=positive integers; N>M).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON-VIET Q. NGUYEN whose telephone number is

(571)270-1185. The examiner can normally be reached on Monday-Friday, alternate Friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Q Nguyen/
Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611